AD-A175 051 THEORETICAL ASPECTS OF VLSI (VERY LARGE SCALE INTEGRATION) CIRCUIT DESIGN(U) MASSACHUSETTS INST OF TECH CAMBRIDGE LAB FOR COMPUTER SCIENCE F T LEIGHTON

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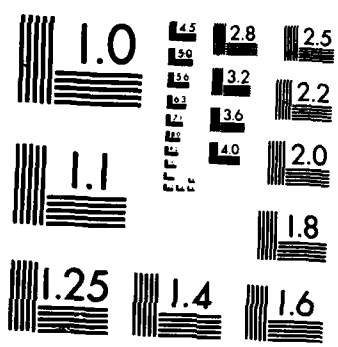

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During the period covered by the grant, two books and ten research papers were written under grant sponsorship. In addition nineteen of the research papers were written and published in conference proceeding. Ten other research manuscripts are now nearing completion. Titles of some of the completed work include: "EIGNENVALUES AND EXPANDERS", A FRAMEWORK FOR SOLVING VLSI GRAPH LAYOUT PROBLEMS", "TIGHT BOUNDS ON THE COMPLEXITY OF PARALLEL SORTING", "WAFER-SCALE INTERGRATION OF SYSTOLIC ARRAYS", and "THE AVERAGE CASE ANALYSIS OF SOME ON-LINE ALGORITHMS FOR BIN PACKING."

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Summary of Research

Our research has been centered in the areas of parallel computation and very large scale integration (VLSI). During the course of the last 3 years, we have identified, formalized and solved several key problems involved in the design of very large scale, very fine grain, high speed parallel computers. The results have had impact in several areas. For example, we developed

1) networks and algorithms for very fast parallel computation,

2) techniques for placement and routing so that the networks can be "laid out" on a chip,

3) algorithms for physical processes such as mask construction so that the chip can be efficiently fabricated, and

4) methods for identifying and overcoming faults introduced during fabrication.

In short, we have dealt with a variety of problems that arise at several steps of the process from design through eventual use.

Our approach to problems in these areas has been largely mathematical. Emphasis was first placed on identifying and formalizing the fundamental issues and problems (e.g., "What networks are best suited for fast parallel computation, and why?") and then on solving the problems using methods and skills from mathematics (particularly combinatorics, probabilistic analysis and asymptotic estimation) and theoretical computer science. Where possible, the results were then applied to the original motivating problem. Most often, this was accomplished by communication of the results to the appropriate applied researchers.

Significant advances were made on a number of specific problems. The most exciting advances were:

1) the discovery of the first N-node, degree-3 network capable of sorting and/or routing any set of N numbers (or packets) in $O(\log N)$ steps using only local control [J7, C11],

2) the construction of the first N-node, degree-3 fixed-connection network capable of simulating any other N-node network or N-processor PRAM with only an $O(\log N)$-factor time delay [J7, C11],

3) the discovery of the first polynomial time (in fact, linear time) algorithm for Manhattan routing that is guaranteed to produce a near-optimal routing for any channel routing problem [J2, C1],

4) the development of methods for converting two-dimensional circuit layouts into more efficient (and nearly optimal) three-dimensional layouts [J9, C14],

5) the proof of superpolynomial lower bounds on the size of fixed-depth PLA's required to compute certain elementary functions [C17],

6) the development of algorithms to decompose vertically convex regions into the minimum possible number of rectangles (with applications to mask design) [C7],

7) the development of several provably efficient algorithms for integrating one- and two-dimensional systolic arrays of functional cells on wafers that contain faulty cells [BC1, J8, C13, C15],

8) the development of the first provably good algorithm for graph bisection, as well as several heuristics that could improve the performance of divide-and-conquer based placement and routing packages [J4, C1],

9) the development of a general theory and method for fault-free placement and routing of arbitrary networks in a two- or three-dimensional medium containing faults [J3, J5, C6],

10) the discovery of the mesh of trees network along with very fast algorithms for arithmetic, linear algebra, graph problems and data manipulation [B1, C12],

11) the proof that bounded width circuits are comparable in power to $NC(1)$ [C2],

12) the proof that monotone circuits for certain graph problems require exponential size [U1],

13) the development of nearly optimal algorithms for multilayer channel routing [U3], and

14) the discovery of optimal layouts for a variety of useful networks including the shuffle-exchange graph and the mesh of trees [B1].

The numbers in brackets refer to the list of papers supported by AFOSR-82-0326. The list is divided into five categories: 1 book [B1], 1 book chapter [BC1], 10 refereed journal publications [J1–J10], 19 papers in conference proceedings [C1–C19], and 10 as yet unpublished manuscripts [U1–U10]. Most of the papers in conference proceedings will eventually appear in refereed journals. The unpublished manuscripts represent our most recent work, and most will eventually appear in conferences as well as refereed journals. Overall, the grant has supported research that has led or will lead to over 50 publications.

Most of the advances listed above have been described in previous reports and requests for renewals. Hence, we will not further elaborate here. Rather, we have included copies of the relevant reprints and preprints at the end of this report. Each paper contains a short abstract and/or introduction that explains the importance and relevance of the work.

Publications Supported by AFOSR-82-0326

Books

1. *Complexity Issues in VLSI: Optimal Layouts for the Shuffle-Exchange Graph and Other Networks,* MIT Press, Cambridge MA, September 1983.

Book Chapters

1. "Algorithms for Integrating Wafer-Scale Systolic Arrays," *VLSI Circuit and Architecture Design,* Ed. Earl Swartzlander, Thurston-Middendorf, to appear.

Refereed Journal Papers

1. N. Alon, "Eigenvalues and Expanders," *Combinatorica,* to appear.

2. B. Baker, S. Bhatt and F.T. Leighton, "An Approximation Algorithm for Manhattan Routing," *Advances in Computing Research: VLSI Theory,* JAI Press, 1984, pp. 205–229.

3. S. Bhatt and F.T. Leighton, "A Framework for Solving VLSI Graph Layout Problems," *J. Computer and System Sciences,* Vol. 28, No. 2, April 1984, pp. 300-343.

4. T. Bui, S. Chaudhuri, F.T. Leighton and M. Sipser, "Graph Bisection Algorithms With Good Average Case Behavior," *Combinatorica,* to appear.

5. F. Chung, F.T. Leighton and A. Rosenberg, "Embedding Graphs in Books: A Layout Problem With Applications to VLSI Design," *SIAM J. Algebraic and Discrete Methods,* to appear.

6. D. Dolev, F.T. Leighton and H. Trickey, "Planar Embeddings of Planar Graphs," *Advances in Computing Research: VLSI Theory,* JAI Press, 1984, pp. 147–161.

7. F.T. Leighton, "Tight Bounds on the Complexity of Parallel Sorting," *IEEE Trans. on Computers,* Vol. C-34, No. 4, April 1985, pp. 344–354.

8. F.T. Leighton and C. Leiserson, "Wafer-Scale Integration of Systolic Arrays," *IEEE Trans. on Computers,* Vol. C-34, No. 5, May 1985, pp. 448–461.

9. F.T. Leighton and A. Rosenberg, "Three-Dimensional Circuit Layouts," *SIAM J. Computing,* to appear.

10. P. Shor, "The Average Case Analysis of Some On-Line Algorithms for Bin Packing," *Combinatorica,* to appear.

Papers in Conference Proceedings

(Most of these papers will eventually appear in final form as refereed journal publications. Those that already have are marked with an asterisk.)

*1. B. Baker, S. Bhatt and F.T. Leighton, "An Approximation Algorithm for Manhattan Routing," *Proc. 15th ACM Symp. on Theory of Computing,* April 1983, pp. 477–486.

2. D. Barrington, "Bounded Width Polynomial Size Branching Programs Recognize Exactly NC^1," *Proc. 18th ACM Symp. on Theory of Computing,* May 1986, to appear.

3. R. Boppana, "Amplification of Probabilistic Boolean Formulas," *Proc. 26th IEEE Symp. on Foundations of Computer Science,* October 1985, pp. 20–29.

*4. T. Bui, S. Chaudhuri, F.T. Leighton and M. Sipser, "Graph Bisection Algorithms with Good Average Case Behaviour," *Proc. 25th IEEE Conf. on Found. of Comp. Sci.,* Oct. 1984, pp. 181–192.

5. J. Buss and P. Shor, "On the Pagenumber of Planar Graphs," *Proc. 16th ACM Symposium on Theory of Computing,* April 1984, pp. 98–100.

6. F. Chung, F.T. Leighton and A. Rosenberg, "Diogenes: A Methodology for Designing Fault-Tolerant VLSI Processor Arrays," *Proc. IEEE Symp. on Fault-Tolerant Computing,* June 1983, pp. 26–31.

7. D. Franzblau and D. Kleitman, "An Algorithm for Constructing Regions with Rectangles: Independence and Minimum Generating Sets for Collections of Intervals," *Proc. 16th ACM Symposium on Theory of Computing,* April 1984, pp. 167–174.

8. A. Goldberg and M. Sipser, "Compression and Ranking," *Proc. 17th ACM Symposium on Theory of Computing,* May 1985, pp. 440–448.

9. S. Goldwasser and M. Sipser, "Arthur Merlin Games versus Interactive Proof Systems," *Proc. 18th ACM Symp. on Theory of Computing,* May 1986, to appear.

10. R. Karp, F.T. Leighton, R. Rivest, C. Thompson, U. Vazirani and V. Vazirani, "Global Wire Routing in Two-Dimensional Arrays," *Proc. 24th IEEE Conf. on Found. of Comp. Sci.,* Nov. 1983, pp. 453–459.

*11. F.T. Leighton, "Tight Bounds on the Complexity of Parallel Sorting," *Proc. 16th ACM Symp. on Theory of Computing,* May 1984, pp. 71–80.

12. F.T. Leighton, "Parallel Computation Using Meshes of Trees," *Proc. 1983 Int. Workshop on Graphtheoretic Concepts in Computer Science,* ed. by M. Nagl and J. Perl, Trauner Verlag, Linz, W. Germany, 1983, pp. 200-218.

*13. F.T. Leighton and C. Leiserson, "A Survey of Algorithms for Integrating Wafer-Scale Arrays," *Proc. MIT Workshop on Wafer-Scale Integration,* Grenoble, France, March 1986, to appear.

14. F.T. Leighton and A. Rosenberg, "Automatic Generation of Three-Dimensional Circuit Layouts," *Proc. IEEE Conf. on Computer Design*, Nov. 1983, pp. 633-636.

15. F.T. Leighton and P. Shor, "Tight Bounds for Minimax Grid Matching, With Applications to the Average Case Analysis of Algorithms," *Proc. 18th ACM Symp. on Theory of Computing*, May 1986, to appear.

16. G. Miller, "Finding Small Simple Cycle Separators for 2-Connected Planar Graphs," *Proc. 16th ACM Symp. on Theory of Computing*, April 1984, pp. 376-382.

17. M. Sipser, "Borel Sets and Circuit Complexity," *Proceedings 15th ACM Symp. on Theory of Computing*, April 1983, pp. 61-69.

18. M. Sipser, "A Complexity Theoretic Approach to Randomness," *Proc. 15th ACM Symp. on Theory of Computing*, April 1983, pp. 330-335.

*19. P. Shor, "The Average Case Analysis of Some On-Line Algorithms for Bin Packing," *Proc. 25th IEEE Symp. on Foundations of Computer Science*, October 1984, pp. 193-200.

As Yet Unpublished Technical Reports and Manuscripts

(Most of these papers will eventually appear as conference papers and/or refereed journal papers.)

1. N. Alon and R. Boppana, "The Monotone Circuit Complexity of Boolean Functions," manuscript, Dec. 1985.

2. D. Barrington, "Width-3 Branching Programs," manuscript, Dec. 1985.

3. B. Berger, M. Brady, D. Brown and F.T. Leighton, "An Almost Optimal Algorithm for Multilayer Channel Routing," manuscript, Dec. 1985.

4. F. Berman, F.T. Leighton, P. Shor and L. Snyder, "Generalized Planar Matching," MIT-VLSI TM #85-234, March 1985.

5. S. Bhatt, F. Chung, F.T. Leighton and A. Rosenberg, "Optimal Embeddings of Binary Trees in the Boolean Hypercube," manuscript, Dec. 1985.

6. R. Boppana, "Approximate Counting for Constant Depth Circuits," manuscript, 1986.

7. R. Boppana, "Levin's Theorem on Pseudo-Random Bit Generators: An Exposition," manuscript, 1986.

8. R. Boppana and J. Lagarias, "One-Way Functions and Circuit Complexity," manuscript, 1986.

9. J. Hastad and F.T. Leighton, "Division in $O(\log N)$ Depth Using $O(N^{1+\epsilon})$ Processors," manuscript, April 1985.

10. M. Sipser, "A Topological View of Some Problems in Complexity Theory," manuscript, 1984.

Copies of Most Significant Papers

In what foilows, we have enclosed copies of the most significant papers supported by AFOSR-82-0326. They are included according to the order in which they are referenced by the preceding list of papers.

END

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